Kevin Chen

(856) 857 – 4373 | kevinchen929@gmail.com
New York Metropolitan Area | linkedin.com/in/kevinchen929

EXPERIENCE

Hudson River Trading | FPGA Verification Engineer | *New York, NY* July 2024 – Present

- Verified ultra-low-latency order entry devices critical to global trading, leveraging open-source tools (cocotb, Verilator) to improve simulation workflows, debug production issues, and collaborate with designers on feature rollouts
- Extended a high-performance C++ testing framework by adding cancel generators to validate device serialization and protected quote generators to verify risk checks and ISO marking, enabling faster iteration on hardware designs
- Implemented fuzzy checks to validate timestamps measuring latency from order arrival to market serialization, improving the team's ability to characterize PNL impact
- Developed a UDP/TCP networking library for communicating with the DUT in end-to-end hardware lab tests
- Built verification support for a message-forwarding mechanism within the device, resulting in latency improvements

Apple | Design Verification Engineer *(Silicon Engineering Group)* | *Cupertino, CA* July 2021 – July 2024

Design Verification Engineer III (Sept 2023 – July 2024)

- Performed power-aware, chip-level verification on 4 chips per year for products like iPhones, iPads, and Macs, working cross-functionally with design, architecture, and firmware teams to integrate over 25 subsystems per chip
- Led chip to power management unit (PMU) co-simulation, delivering a software model used by dozens of engineers to run over 1,000 end-to-end integration tests with clock gating, power gating, and accurate power rail sequencing
- Coordinated inter-team discussions for major architectural updates to the chip and PMU state machines, meeting with stakeholders as my team's subject matter expert to establish comprehensive verification requirements
- Bolstered the CI/CD pipeline with directed tests validating the chip's power state transitions and randomized test sequences cycling through various states to ensure comprehensive coverage, debugging failures as they arose

Design Verification Engineer II (July 2021 – Sept 2023)

- Developed and drove global adoption of new coverage tools, parsing Excel and JSON databases to generate assertions and covergroups enforcing design invariants; accelerated bug detection by 2–3 months at the unit level
- Implemented abstractions used by dozens of engineers to expedite their transition to a new regression framework, collaborating with DevOps/Tooling teams to focus on user experience and make the transition as seamless as possible
- Drove the validation of chip power states by writing integration tests that simulate typical user behavior, engaging with firmware teams to receive sequence deliveries, and spearheading debugs to confirm the chip behaves as expected

Penn Electric Racing | Electrical Lead | *University of Pennsylvania* Sept 2017 – May 2021

- Led a 25 member team, designing custom electronics for racecars that place top 3 internationally at FSAE Lincoln
- Oversaw the printed circuit board (PCB) development schedule, conducting design reviews, authorizing all board layouts, and ensuring timely procurement of about 15 complex four-layer boards with over 2000 components annually

EDUCATION

University of Pennsylvania, School of Engineering & Applied Science | Philadelphia, PA May 2021

MSE in Electrical Engineering | **BSE** in Computer Engineering **GPA:** 3.90/4.00

Minors: Mathematics, Engineering Entrepreneurship Summa Cum Laude ('21) | Tau Beta Pi ('20)

Course projects can be found at www.kevinjchen.me

SKILLS

- **Software**: Python (cocotb) | C/C++ || *Working Knowledge*: Linux | bash
- **Hardware**: SystemVerilog/Verilog (*exposure to* UVM) | Waveforms (Verisium/Indago, Verdi) | UFP | Tcl
- **Misc**: PCB Design (Altium) | Electronics Lab Equipment | Version Control (Git, Perforce)