Kevin Chen

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EXPERIENCE

Hudson River Trading | FPGA Verification Engineer | *New York, NY* July 2024 – Present

- Leveraged open source environments (Cocotb, Verilator) to verify ultra-low latency products that support trading on global markets, collaborating with designers for rapid bring up of new projects and debug of existing designs

Apple | Design Verification Engineer (*Silicon Engineering Group*) | *Cupertino, CA* July 2021 – July 2024

Design Verification Engineer III (Sept 2023 – July 2024)

- Performed chip-level verification on 4 chips per year for use in products like iPhones, iPads, and Macs, working cross-functionally with design, architecture, and firmware teams to integrate over 25 subsystems per chip
- Developed and drove the global adoption of new software debugging tools, used by component-level developers in unit testing to detect bugs 2-3 months earlier; also developed tools that improved test coverage, parsing Excel and JSON databases to automatically generate assertions enforcing design invariants
- Owned chip to power management unit (PMU) co-simulation, delivering a software package to dozens of engineers that allowed over 1000 tests perform end-to-end testing with accurate power rail sequencing events
- Bolstered the CI/CD pipeline with integration tests that validated the chip's power state transitions and ad hoc regressions that cycled through random states to ensure comprehensive coverage

Design Verification Engineer II (July 2021 – Sept 2023)

- Coordinated inter-team discussions for major architectural updates to the chip and PMU state machines, meeting with stakeholders as my team's subject matter expert to establish comprehensive verification requirements
- Implemented abstractions used by dozens of engineers to expedite their transition to a new regression framework, working with DevOps/Tooling teams to focus on user experience and make the transition as seamless as possible
- Drove the validation of chip power states, writing integration tests that simulate typical user behavior, engaging with firmware teams to receive sequence deliveries, and spearheading debugs to confirm the chip behaves as expected

Penn Electric Racing | Electrical Lead | *University of Pennsylvania* Sept 2017 – May 2021

- Led a 25 member team, designing custom electronics for racecars that place top 3 internationally at FSAE Lincoln
- Oversaw the printed circuit board (PCB) development schedule, conducting design reviews, authorizing all board layouts, and ensuring timely procurement of about 15 complex four-layer boards with over 2000 components annually
- Engineered a semi-distributed 300V battery management system, equipped with daughter boards for precise battery monitoring and a central motherboard that acts on the data, resulting in no injuries or battery failures

Relativity Space | Avionics Power Intern | *Los Angeles, CA* Summer 2020

- Advanced first flight readiness by engineering a battery management system critical to both stages of the final rocket
- Co-routed a 16-layer power distribution board, cutting the development timeline by over half a month

EDUCATION

University of Pennsylvania, School of Engineering & Applied Science | Philadelphia, PA May 2021

MSE in Electrical Engineering | **BSE** in Computer Engineering **GPA:** 3.90/4.00

Minors: Mathematics, Engineering Entrepreneurship Summa Cum Laude ('21) | Tau Beta Pi ('20)

Course projects can be found at www.kevinjchen.me

SKILLS

- **Software**: Python | C/C++ | Linux | Version Control (Perforce, Git) || *Working Knowledge*: Perl | Java | bash | SQL
- **Hardware:** Waveform Debug (Verisium, Verdi) | Verilog/SystemVerilog (*exposure to* UVM) | UPF | Tcl
- **Electrical Engineering:** PCB Design (Altium) | Electronics Lab Equipment | Soldering | Embedded Platforms